SPECIFICATION AMENDMENTS

Please amend the specification by replacing the paragraph below.

[0161] The sense module shown in **FIG. 6A, FIG. 10 and FIG. 14** is preferably implemented in a memory architecture configured to perform all-bit-line sensing. In other words, contiguous memory cells in a row are each connectable to a sense module to perform sensing in parallel. Such a memory architecture is also disclosed in co-pending and commonly assigned United States patent application Serial No. 10/254,483 filed September 24, 2002, entitled "Highly Compact Non-Volatile Memory And Method Thereof," by Raul-Adrian Cernea, published as 2004-0060031-A1. The entire disclosure of said patent application is hereby incorporated herein by reference.